# Ming-Hong Lin

Taipei,Taiwan

(+886)960013156 harry2963753@gmail.com akira2963753 Ming-Hong, Lin

## EDUCATION

**National Taiwan University of Science and Technology** *Feb. 2026 - Present*

*M.S. in Electrical Engineering (Integrated Circuits and Systems)*

**National Taiwan University of Science and Technology**

*B.S. in Electrical Engineering (Integrated Circuits and Systems)* *Sept. 2022 - Dec.2025*

- GPA : 4.03/4.30
- Rank : 28/158 (17.95%)
- Selected Course : Digital System Design (A+), Digital System Design Practicum (A+), Introduction to VLSI Designs (A+), Computer Organization (A+), FPGA System Design and Practicum (A+)

## WORK EXPERENCE

**FPGA Digital IC Design Intern at Ranictek** *Sept. 2025 - Present*

- Developed LDPC algorithms and designed encoder/decoder IP cores

## PROJECT

**Low-Cost & High-Performance AI Accelerator Based on Google's TPU** *Feb. 2025 - Oct. 2025*

- Reduced memory access by 18.46% and systolic-array overhead by 16.4%, improving 6.54 TOPS
- Improved accuracy by 0.1–0.6% compared with standard INT8 quantization

**Five-Stage Pipelined RISC-V CPU on FPGA**

- Supported RV32I/RV32M and implemented 2-way set-associative caches with an AXI-to-BRAM
- Included forwarding, hazard detection and dynamic branch prediction unit

**LDPC Encoder & Decoder on FPGA Based on IEEE 802.11n**

- 250 MHz LDPC Encoder using the Richardson–Urbanke algorithm and Decoder supporting code rates 1/2 and 2/3

## CONTEST & CONFERENCE EXPERIENCE

**11th Taiwan and Japan Conference on Circuits and Systems (TJCAS 2025)**

*Shyue-Kung Lu, Yu-Xian Huang, **Ming-Hong Lin** and Chia-Hung Hsiao, "Weight-Aware and Reduced-Precision Architecture Designs for Low-Cost AI Accelerators"*

**4th International Practical Applications Seminar on Electrical Engineering and Computer Science**

***Ming-Hong Lin**, Chia-Hung Hsiao and Shyue-Kung Lu, "Low-Cost and High-Performance AI Accelerator Architecture Design Based on Weight Characteristics"*

## SKILLS

**IC Design Skills:** System Modeling & Algorithms,, RTL Design, Logic Synthesis, APR, FPGA System Design
**Design Tool:** ModelSim, Vivado, Design Compiler, IC Compiler
**Programming Languages:** Verilog, SystemVerilog (Basic), Python, C/C++ (Basic)
**Languages:** Mandarin (native), English